REMARKS

Claims 1-10, 12-23, 25-26, and 51-80 are now pending in the application. Claims 11, 24, and 80-85 are cancelled without disclaimer or prejudice to the subject matter contained therein. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 102

Claims 1-11, 14-24, 57-58, and 60-85 are rejected under 35 U.S.C. § 102(b) as being anticipated by Jaggar (U.S. Pat. No. 5,701,493). This rejection is respectfully traversed.

With respect to claim 1, Jaggar fails to show, teach, or suggest a register file for a data processing system comprising input ports to receive inputs for addressing at least one of the memory locations using an encoded address and an address encoder for each of the input ports, the address encoder to provide an encoded address for accessing one of the memory locations. In contrast, Jaggar appears to disclose a single alleged address encoder for all of the input ports of a register.

For anticipation to be present under 35 U.S.C §102(b), there must be no difference between the claimed invention and the reference disclosure as viewed by one skilled in the field of the invention. Scripps *Clinic &* Res. *Found. V. Genentech, Inc., 18* USPQ.2d 1001 (Fed. Cir. 1991). All of the limitations of the claim must be inherent or expressly disclosed and must be arranged as in the claim. *Constant v.*

Advanced Micro-Devices. Inc., 7 USPQ.2d 1057 (Fed. Cir. 1988). Here, Jaggar fails to disclose an address encoder for each of the input ports.

As shown in an exemplary embodiment in FIG. 4, a register file 206 includes a register file memory unit 400 and a plurality of address encoders including, for example, address encoders 402_1, 402_2, 4023, 402_4, 4101, and 410_2. Each of the address encoders receives a plurality of inputs. For example, the address encoder 402, receives a processor mode input and a srcl.index input. In other words, each of the inputs to the register file memory unit 400 includes a corresponding address decoder.

As best understood by Applicants, Jaggar does not disclose this limitation. For example, with respect to claim 11, the Examiner alleges that Jaggar discloses "an address encoder to provider an encoded address" (emphasis added), relying on "the combination of components 12-20 in Fig. 8." Applicants respectfully note that FIG. 8 of Jaggar does not disclose an address encoder for **each** of the input ports as claim 1 recites. Instead, as best understood by Applicants, FIG. 8 of Jaggar discloses a single alleged address encoder (i.e. the components 12-20) for all of the registers.

Applicants respectfully submit that claim 1, as well as its dependent claims, should be allowable for at least the above reasons. Claims 14, 51, 64, 74, and 78, as well as their corresponding dependent claims, should be allowable for at least similar reasons.

Applicants respectfully note that the amendments to claim 1, as well as claims 51, 64, 74, and 78, include subject matter that was previously presented in at least cancelled claims 11 and 24. As such, Applicants respectfully submit that these

amendments do not represent new matter and respectfully request that the Examiner consider the claims in view of these amendments.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

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